IN THE CLAIMS

The following is a clean version of the entire set of pending claims. Claims that are shown in *italics* are not amended. In accordance with 37 C.F.R. §1.121(c)(1)(ii), Attachment A provides a marked-up version of the claims containing the newly introduced changes.

Please cancel Claim 1 without prejudice or disclaimer.

Please cancel Claim 2 without prejudice or disclaimer.

Please cancel Claim 3 without prejudice or disclaimer.

4. (Amended) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment signal being filtered,

wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input,

and wherein the output of the at least one coefficient circuits is to a delay and the output of delay sent to the at least one coefficient circuits.

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5. (Amended) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment signal being filtered,

wherein the second circuit includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input,

and wherein the coefficient circuit includes an input summer and a coefficient multiplier.

Please cancel Claim 6 without prejudice or disclaimer.

Please rewrite Claim 7 to read as follows:

7. (Amended) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element,

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and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of an output without the adjustment signal being filtered,

wherein the first input and output are phase representations and wherein the adjustment input causes an integer multiple of 2π shift in the output signal.

Please cancel Claim 8 without prejudice or disclaimer.

Please cancel Claim 9 without prejudice or disclaimer.

10. (Amended) A circuit comprising:

a first circuit portion connected to a first input, the first circuit portion including at least one delay element; and

a second circuit portion attached to the first circuit portion, the second circuit portion including at least one delayed signal input from the at least one delay element, and an adjustment input, the adjustment input not passing through the at least one delay element, wherein when there is no adjustment input, the circuit acts as a filter, and wherein the adjustment input changes the level of the output without the adjustment being filtered; and

adjustment control logic adapted to provide the adjustment input,

wherein the adjustment control logic is adapted to produce a minus 2π adjustment signal if a tested signal is greater than a positive reference value and

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produce a positive 2π adjustment signal if the tested signal is less than a negative reference value.

Please cancel Claim 11 without prejudice or disclaimer.

12. A circuit comprising:

a digital filter including input lines giving signal values at different time indexes, coefficient multiplier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the coefficient multiplier circuitry to produce an output value; and

summing circuitry connected to the input lines of the signal values at different time indexes and to an adjustment input, wherein the output of the summing circuitry being sent to the coefficient multiplying circuitry.

Please rewrite Claim 13 to read as follows:

13. (TwiceAmended) A method comprising:

providing a circuit;

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inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit;

inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset that is added at the output; and

adding the adjustment signal to the input signal.

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14. The method of claim 13, wherein the adjustment signal keeps the output within a preset range.

15. The method of claim 13, wherein the filtering of the input signal is a low-pass filtering.

16. The method of claim 13, wherein the input is a phase signal.

17. The method of claim 13, wherein the input is a hue signal.

Please rewrite Claim 18 to read as follows:

18. (Amended) A method comprising:

constraining a phase signal within a finite preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal.

19. The method of claim 18, wherein the filtering of the modified phase signal is a low-pass filtering.

Please rewrite Claim 20 to read as follows:

20. (Amended) A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

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filtering the phase signal without filtering the correction signal portion of the phase signal

wherein the correction signal is an integer multiple of 2π.

Please rewrite Claim 21 to read as follows:

21. (Amended) A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal

wherein the preset range is zero to 2π.

Please rewrite Claim 22 to read as follows:

22. (Amended) A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal

wherein the preset range is zero to 2π plus a guard band.

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23. The method of claim 22, wherein the guard band is a reference value above or below the range zero to 2π.

24. The method of claim 23, wherein the guard bands are -π to zero and 2π to 3π.

25. The method of claim 18, wherein the constraining step is such that the phase signal is processed so as to use a differential input.

Please rewrite Claim 26 to read as follows:

26. (Amended) A method comprising:

constraining a phase signal within a preset range, the constraining step including adding a correction signal to the phase signal; and

filtering the phase signal without filtering the correction signal portion of the phase signal

wherein the constraining step is such that the phase signal is processed so as to use a differential input and wherein the differential input is offset by an integer multiple of 2π so as to reduce the absolute value of the differential input.

27. The method of claim 18, wherein the phase signal is a hue signal.

Please rewrite Claim 28 to read as follows:

28. (Twice Amended) An apparatus comprising:

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circuitry to constrain a phase signal within a finite preset range using a correction signal; and

a filter adapted to filter the phase signal without filtering the correction signal contribution, and to add the correction signal to the phase signal.

29. A method of processing data for video comprising:

providing picture data including hue information encoded as a phase having a first range;

producing a filtered hue information signal, the filtered hue information signal including unfiltered offsets of plus or minus 2π.

30. The method of claim 29, wherein producing a filtered hue information signal including adding the unfiltered offsets to the hue information signal.

31. An electronic circuit comprising:

a delay which receives an input signal and outputs a delayed input signal;

a first adder which outputs a first corrected signal by adding a correction signal to the input signal;

a second adder which outputs a second corrected signal by adding the correction signal to the delayed input signal; and

a third adder which outputs an output signal by adding the first corrected signal and the second corrected signal.

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